William Malcolm Bauer

TRANSISTOR BIAS CIRCUITS.

Research paper no. 17.

UNITED STATES
NAVAL POSTGRADUATE SCHOOL

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-BY-

WM. MALCOLM BAUER
Professor of Engineering Electronics

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Professor of Engineering Electronics

U. S. Naval Postgraduate School
Monterey, California

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BIAS and STABILIZATION

W. M. Bauer

As with tubes, transistors must be put into the proper operating condition by means of DC biasing. The collector junction must be reverse biased with a voltage from a battery or power supply. A load is in this circuit. The emitter junction must be forward biased with current. For amplifier or control action, this current is varied by the signal, with the result that the current in the load circuit is similarly varied.

Our first consideration is the circuitry which will provide the desired biasing.

I. Common Base Circuit: Figure 1 shows the method of biasing a common base amplifier. As figure 2 shows, the choice of the DC operating Q-point may be dictated by the amount of output voltage or current swing that is desired. For maximum undistorted output voltage swing, plus and minus, $R_L = \frac{.5E}{I_e}$. But if small signal operation is employed, then the value of R_L would be dictated by the desired gain. The Q-point may then be selected at will, and may be at rather low collector voltage and current. For a small transistor the collector voltage might be a few volts, and the emitter current a milliampere or less.

The emitter bias current must be obtained from a separate battery, and the series resistance R_e is given the value which will pass the desired biasing current. $R_e = \frac{E_e - .15}{I_e}$. If the signal is capacitively coupled to the emitter, then R_e shunts the input resistance of the

transistor. But as this is of the order of 40 ohms, it ordinarily does not require much emitter supply voltage to make Re sufficiently large. If the secondary of a driver transformer is connected in series with the emitter, R_e will decrease the input signal unless this resistor is bypassed. If the source is of low impedance, then only a portion of R_e should be bypassed. The non-linear diode forward-characteristic must be swamped by a sufficiently large linear resistance, either in the primary or secondary of the input transformer.

II. <u>Common Collector Circuit</u>: Figure 3 is a biasing circuit for a grounded collector amplifier, and figure 4 shows this circuit turned over. This circuit is an emitter-follower, like the cathode-follower tube circuit. Only one battery is needed since the biasing voltage between collector and base is of the right polarity to supply the biasing current for the base. The value of $R_3 = \frac{V_{bc}}{I_b}$, where V_{bc} is selected upon the same considerations as in part I. The value of I_b is chosen when the Q-point on the common-emitter collector-current characteristics is decided on. R_3 will be an AC shunt to the input resistance of the common collector amplifier if the signal is capacitively coupled to the base. To make R_3 large, V_{cb} should be large, and the base current small. A small value of load current will require only small base current. A high β transistor will require less base current.

If an input transformer supplies the signal current in series with R_3, R_3 may be completely bypassed since the input resistance of the emitter follower has been linearized by the load resistance. In

this case no effort need be made to make R_3 large.

III. <u>Common Emitter Circuit</u>: Figure 5 is the obvious way to bias the common emitter amplifier. For this and the previous circuit, the bias input current is the base current. It may seem unnatural to consider base current as an independent variable, since in the common base circuit the emitter current is the independent variable. Considering figure 6, a slight forward biasing voltage, V_{be}, causes an emitter junction injection of current into the base. Something like 95% of this current flows into the collector and is returned through the aid of the collector battery to the emitter. The small 5% fraction of the injected current flows out the base lead. If the forward biasing voltage is increased, the emitter current and base current increase by the same proportion. Thus base current may be the independent variable. The base current receives both DC and AC amplification, of nearly β, by transistor action.

Because the collector supply voltage is of the same polarity as the base biasing battery in figure 5, the collector supply voltage itself may supply the base bias current, as in figure 7. $R_3 \cong \frac{E}{I_b}$, will be a very high resistance and so with capacitive coupling it will scarcely rob the transistor of any input current.

Figure 8 uses the collector voltage itself, to provide the base current bias through R_3. This is called self-biasing.

Figure 9 is another means of biasing a common emitter circuit. It differs from figure 7 only in having resistor R_1 in the battery circuit.

Figure 10 is for transformer drive. The $I_e \cdot R_1$ voltage drop must be less than E_1 to send the bias current through the transistor (about .15 volt) and through the resistance R_2 of the secondary. The base potential will be $I_b \cdot R_2$. I_b is determined by the transistor type and the chosen Q-point. $R_1 = \frac{E_1 - V_b - .15}{I_e}$

Another base biasing method is that of figure 11. The voltage divider, R_3R_2 may be such as to provide the proper value of base current, which is the difference of currents I_3 and I_2. $R_L + R_1$ may be determined by selection of the Q-point. For maximum output, $R_L + R_1 \doteq \frac{V_{cb}}{I_e}$. R_1 may be selected, such as 500 or 1000 ohms, or V_b may be assigned a value, perhaps, a tenth of E. Then $R_1 = \frac{.1E}{I_e}$. R_L is now obtained. Next I_2 could be allowed to be, say, .3 or .5 of I_e. I_3 is then $I_2 + I_b$. $V_3 = E - V_b$, and so R_2 and R_3 can be computed. These two bias resistors are both shunting the high input impedance of the transistor between base and ground, so that for capacitive coupling of the signal to the base, there may be considerable shunting of AC signal current away from the transistor.

Figure 12, like figure 8, connects R_3 to the collector. The design of component values may proceed much as above.

$$R_3 = \frac{E - V_b - (I_e + I_2)\,R_L}{I_2 + I_b} \doteq \frac{.5E}{I_2 + I_b}$$

It may be difficult to make R_3 at least five times R_L.

SELECTION OF A BIAS CIRCUIT

The common emitter circuit offers a choice from seven circuits, figures 5, 7, 8, 9, 10, 11, 12. Already the shunting effect of some of these for AC signal has been mentioned. Another consideration is whether the bias circuit gives feedback, and whether it is desired or must be eliminated. One most important consideration is whether the bias circuit provides temperature stabilization. A circuit which must operate under widely different values of transistor temperature must be stabilized against changes of the Q-point caused by changes of the reverse saturation current, I_{co}.

Only a brief consideration of feedback will be attempted at this point since another chapter treats this topic. Negative AC feedback is apparent in figures 3, 4, 8, 9, 10, 11 and 12. The common collector, like the cathode follower, has 100% voltage feedback due to the load. Negative AC current feedback, due to the emitter degeneration of the bias resistor R_1, appears in figures 10, 11 and 12. In figures 8 and 12 there is negative AC voltage feedback from collector to base via bias resistor R_3. This feedback may be eliminated by tapping a bypass capacitor near the center of R_3 to ground. Emitter bypassing may be employed in figures 10, 11 and 12. R_1 may be bypassed in figure 9.

Q-POINT STABILIZATION

The theory of the reverse saturation current across the collector junction was given in chapter 1. Problem 1 of that chapter showed how this current, called I_{co}, increases with temperature. Figure 13 shows the experimentally observed dependence of I_{co} in germanium upon

temperature. I_{co} doubles for every 10° or 11° centigrade increase of temperature. The same is true of silicon, but this current is of a lower order of magnitude. The temperature generation of current across the collector junction adds a DC constant current generator, I_{co}, in parallel with the DC constant current generator αI_e; see figure 15. This is shown by the collector characteristics of the common base circuit, and by the equation $I_c = I_{co} + \alpha I_e$. Temperature has only slight effect on α, so the increase of I_{co} with temperature shifts all of the collector characteristic curves of the common base circuit upward by the increase of I_{co}. This increase is microamperes, and so if I_e is of the order of a milliampere, the shift of the Q-point is of no real significance since I_e is a fixed bias current in the common base circuit.

For the common emitter circuit, the equation for I_c with fixed collector voltage is, from the chapter on characteristics,

$$I_c = \frac{I_{co}}{1 - \alpha} + \beta I_b$$

With a value such as .02 for $1 - \alpha$, the temperature effect on the collector characteristic curves is very marked. This is shown in figure 14. For the common emitter circuits of figures 5 and 7 the bias current to the base is fixed, independent of temperature. As a result, there is no stabilizing reaction and the Q-point shifts with the intersection of the curve for the fixed value of I_b, and the load line. This is shown in figure 14. There are two reasons for trying to prevent shift of the Q-point. The shift will reduce the maximum

undistorted output swing. The transistor parameters which control gain, change considerably with shift of the Q-point. So, to stabilize the amplifier performance, the Q-point should not be permitted to wander around on the I_c - V_{ce} plane. It is obvious then that the base bias current must be automatically reduced as temperature increases. Another way to say this is that the bias circuit should have DC negative feedback.

Consider the self-bias circuit of figure 8. As I_c increases with temperature, the collector voltage drops, and I_b drops in the same proportion. This is a DC negative voltage feedback dependent on the DC resistance of the load. Similar action occurs in figure 9. Emitter degeneration due to R_1 in figures 10, 11 and 12 is, like cathode degeneration, negative DC current feedback. Thus R_1 provides temperature stabilization of the Q-point .

STABILIZATION FACTOR

It will be sufficient to analyze the circuit of figure 12, since all the others are special cases of this circuit. For example, figure 8 comes from figure 12 if $R_1 = 0$ and R_2 is infinite.

Analysis of the self-bias double-mesh circuit: In figure 12 the $I_e R_1$ voltage is large relative to the forward bias voltage drop of the transistor from emitter to base. This allows us to neglect the emitter to base voltage, hence we may consider R_1 and R_2 in parallel. Furthermore, this forward bias voltage will remain fairly constant as I_e and I_b vary due to temperature. We are concerned with the changes of all quantities such as I_e, I_b, and I_c, as I_{co} increases with temperature.

Thus we wish to analyze the incremental circuit of figure 15 in which the constant battery voltage and the nearly constant emitter-base voltage drop are omitted. This is similar to the AC equivalent circuit, as is familiar in tube work. The two constant DC current generators across the collector junction are the equivalent of the transistor. It is noted that the increment of I_{co} is supplied in part by the decrement of base bias current, ΔI_b, and the remainder by $(1 - \alpha) \Delta I_e$. Our object is to make this latter contribution to ΔI_{co} as small as possible. If ΔI_b could supply the entire amount of ΔI_{co}, then ΔI_e would be zero. In this case, like the common base circuit, the increment of the collector current is ΔI_{co} only. For transistors of high β, the ΔI_e must be large to supply the small $(1 - \alpha) \Delta I_e$ component of ΔI_{co}. Thus stabilization is more necessary for high β transistors.

Since R_1 and R_2 are in parallel,

$$\Delta I_2 = \frac{\Delta I_e R_1}{R_2} \tag{1}$$

$$\Delta I_L = \Delta I_e + \Delta I_2 = \Delta I_e \left(1 + \frac{R_1}{R_2}\right) \tag{2}$$

$$\Delta I_3 R_3 = \Delta I_e R_1 + \Delta I_L R_L \tag{3}$$

$$\Delta I_3 = \Delta I_e \left[\frac{R_1 + \left(1 + \frac{R_1}{R_2}\right) R_L}{R_3}\right] \tag{4}$$

$$\Delta I_b = \Delta I_2 + \Delta I_3 = \Delta I_c - \Delta I_e \tag{5}$$

$$\Delta I_c = \Delta I_{co} + \alpha \Delta I_e \tag{6}$$

Now substitute 1, 4 and 6 into 5.

$$\frac{\Delta I_e}{\Delta I_{co}} = \frac{1}{1 - \alpha + \frac{R_1}{R_2} + \frac{R_1}{R_3} + \frac{R_L}{R_3}\left(1 + \frac{R_1}{R_2}\right)} \qquad (7)$$

The degree of stabilization provided by the circuit is measured by this equation. The rate of change of emitter current with respect to reverse saturation current is called the current stabilization factor.

$$S_i = \frac{\Delta I_e}{\Delta I_{co}} \qquad (8)$$

The degree of excellence of stabilization is indicated by the smallness of S_i. Optimum stabilization would have $S_i = 0$, meaning that the entire increment of I_{co} is supplied by the decrement of I_b. A value of $S_i = 5$ might be considered a pretty well stabilized circuit.

A qualitative analysis of the circuit of figure 15 tells us that to make ΔI_b large, R_1 should be large and R_2 small to make ΔI_e small and ΔI_2 large. Also large R_L and small R_3 make ΔI_3 large. These relative resistance values in equation 7 will make S_i small.

By comparing the common base circuit figure 1 with the self-bias double-mesh bias circuit of figure 12, it may be shown that equation 7 gives $S_i = 0$.

Similarly for the common collector circuit figure 4, equation 7 reduces to

$$S_i = \frac{1}{1 - \alpha + \frac{R_L}{R_3}} \qquad (9)$$

In this circuit R_L may be small, and R_3 is very large, so the Q-point

of the emitter follower is not well stabilized.

The two fixed bias circuits for figures 5 and 7 require the entire increment of I_{co} to be supplied by $(1 - \alpha) \Delta I_e$ and hence have no stabilization other than that provided by the α value of the transistor. Equation 7 reduces to

$$S_i = \frac{1}{1 - \alpha} = \beta + 1 \tag{10}$$

The incremental self-bias circuit of figure 8 is identical with that of the emitter follower, and equation 9 also applies. The higher the β of a transistor, the larger R_3 must be because of smaller base current, and so the circuit does not provide much stabilization, especially where it is needed.

The two-battery circuit of figure 10 has an incremental circuit like that of figure 15 except that R_3 is infinite.

Thus $$S_i = \frac{1}{1 - \alpha + \frac{R_1}{R_2}} \tag{11}$$

The last of the common emitter bias circuits is the double mesh circuit of figure 11. Its incremental circuit is shown in figure 16 and is identical with that of the two battery circuit, figure 10, if the parallel resistance of R_3 and R_2 replaces R_2 of figure 10. Thus

$$S_i = \frac{1}{1 - \alpha + R_1\left(\frac{1}{R_2} + \frac{1}{R_3}\right)} \tag{12}$$

Since $$I_c = \alpha I_e + I_{co}$$

$$\frac{dI_c}{dI_{co}} = \alpha \frac{dI_e}{dI_{co}} + 1$$

$$\Delta I_c = (\alpha S_i + 1) \Delta I_{co} \tag{13}$$

And since $$I_c = \frac{I_{co}}{1-\alpha} + \beta I_b$$

$$\frac{dI_c}{dI_{co}} = \frac{1}{1-\alpha} + \beta \frac{dI_b}{dI_{co}}$$

Thus $$\Delta I_b = \left[(1-\alpha) S_i - 1\right] \Delta I_{co} \tag{14}$$

The increments of collector and base biasing currents may be calculated by equations 13 and 14. It is to be noted that if ideal stabilization is achieved for which $S_i = 0$, then $\Delta I_b = -\Delta I_{co}$. That is, in figure 15, since the entire increment of I_{co} is supplied by the decrement of I_b, ΔI_e is zero.

It is entirely possible for ΔI_b to be larger than I_b, especially when I_b is a small value. The result is that the direction of the biasing base current reverses. This is to be seen by the curves of figure 14. If the Q-point is well stabilized on the collector characteristic plane, the upward shift of the characteristic curves may carry the $I_b = 0$ line above the Q-point. Is transistor action lost when this occurs? No. The amplifier action of the transistor still continues as the signal, of reversed base current, reduces I_c. The limit however is when I_c has been reduced to I_{co}. When I_{co} is large and when I_e is small, then $(1-\alpha) I_e$ is insufficient to supply I_{co}, and so I_b must reverse to help out. The maximum instantaneous reverse base current is I_{co}. The maximum negative swing of base signal current is thus, $I_b + I_{co}$.

DIRECT COUPLED STAGES

Two common emitter transistor direct coupled stages are shown in figure 17. The first stage is fairly well stabilized by the double mesh circuit of figure 11, for which equation 12 gives the stabilization factor. The ΔI_{c1} may be calculated by equation 13. This increment divides between the load and the next stage. The ΔI to the second stage splits into ΔI_2 and ΔI_b, as shown in figure 17. By proper choice of resistor values, it is possible for complete stabilization of the second stage. That is, the ΔI_b supplied by the first stage may supply the entire increment of I_{co} required by the second stage. In this $\Delta I_{c2} \approx \Delta I_{co}$. If ΔI_b is a bit larger, then ΔI_{c2} could be made zero.

THERMAL RUNAWAY

The biasing circuit of figure 18 is particularly susceptible to a thermal regenerative increase of heat generation which results in destruction of the transistor. The base current is fixed, and the collector voltage is nearly the battery voltage. The watts of electrical power converted into heat inside the transistor at the collector junction is

$$P_d \approx EI_c \approx E \left[\beta I_b + \frac{I_{coa}}{1 - \alpha} \epsilon^{b(T_j - T_a)} \right] \qquad (15)$$

where I_{coa} is the reverse saturation current at ambient temperature. The actual I_{co} is greater than this because the junction temperature is above ambient due to power dissipation. The slope of the I_{co} curve of figure 13 gives $b \approx 2.3026 \ (\log 100 - \log 10) \div 37 \approx .0624$ and so I_{co} at junction temperature is given as shown in equation 15.

The power dissipated inside the transistor increases exponentially with time after closing the circuit. Perhaps at some elevated temperature the rate of heat flow out equals the rate of internal heat production. This stable equilibrium condition is shown in figure 19 for both an ambient temperature of 10° and 30° C. The rate of heat flow away from the transistor is assumed proportional to the difference between the junction temperature and ambient temperature, and so is shown by a straight line from ambient temperature. At ambient temperature of 50° C, figure 19 shows no stable intersection can be obtained. The heat conduction away is less than the heat production so the temperature increases indefinitely which damages the transistor. Since the heat storage capacity of a transistor may be small, the thermal runaway can be so rapid that an observer must be quick on the switch to prevent damage to a meter in the circuit.

Thermal runaway could be avoided for a 50° C ambient in figure 19 if better thermal contact could be made with a good heat sink. This would steepen the heat loss line to provide a stable intersection. Thermal runaway is more apt to occur if the transistor is biased to large currents. Good stabilizing bias circuits prevent thermal runaway by automatically reducing I_b as the I_{co} at junction temperature increases.

The thermal effect is what prevents one from obtaining a set of static characteristics by the direct point by point DC method. A pulse method is employed by characteristic curve tracers.

Problem 1. Show that $\Delta I_e \cong \Delta I_{co}$ for the common base circuit by identifying its incremental circuit with that of figure 15 when some resistors are zero or infinite. Substitute in equation 7.

Problem 2. Derive equations 9 and 10.

Problem 3. What is the equation for S_i in figure 9.

Problem 4. A transistor has $I_{co} \cong 5$ microamperes at 20° C and it has an $\alpha \cong .980$. It is to be used in the self-bias double mesh stabilization circuit of figure 12. The load resistance $R_L \cong 2$ k, and let $R_1 = 1$ k. Select $I_e \cong 1$ ma and $V_{ce} \doteq 5$ v. Let $I_2 \cong .1$ ma.

a. Find battery voltage E, and resistance R_2.

b. Find I_c, and I_b, and R_3.

c. Calculate the stabilization factor S_i.

d. Due to increase of temperature to 45° C, I_{co} increases by 20 microamperes. Find the new values of I_c and I_b.
Is the maximum undistorted output current less than at 20° C?

e. Show connections and polarities of electrolytic bypass capacitors to eliminate AC feedback.

Problem 5. A transistor at room temperature has $I_{co} = 3.7$ microamperes. In the circuit of figure 20, a current of 74.5 microamperes flows. Find the increment of temperature above room temperature at which the amplifier will cease to function satisfactorily for even the smallest signal.

Problem 6. The stabilization factor of the common collector circuit may be reduced by the circuit of figure 21, as compared with figure 3.

a. Reduce equation 7 to obtain S_i for this circuit by comparison with figure 12.

b. Discuss the advantage of using a large resistor for R_L when the actual load is capacitively coupled to the emitter and is a smaller resistance.

c. Discuss the purpose in connecting a capacitor between the junction of R_4 and R_5 and the emitter. Could this same idea be applied to any common emitter circuit?

d. Design the DC circuit using a 2N43 transistor at $V_{ce} = -10$ v using a 30 v power supply. Let $I_b = 50$ microamperes and I_c is 3.0 ma. Let R_4 be 10 k, and let I_5 be .25 ma. Compute S_i.

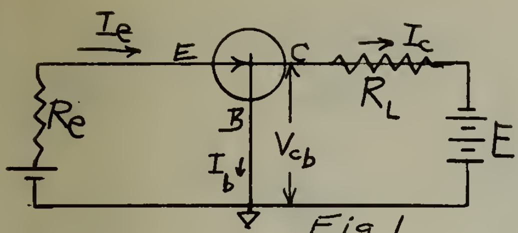

Fig. 1

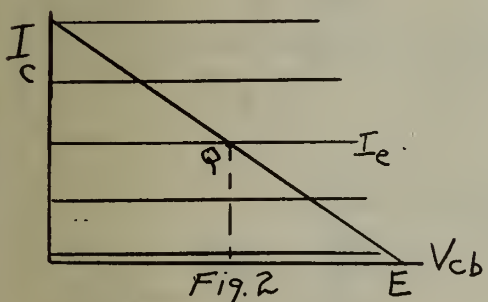

Fig. 2

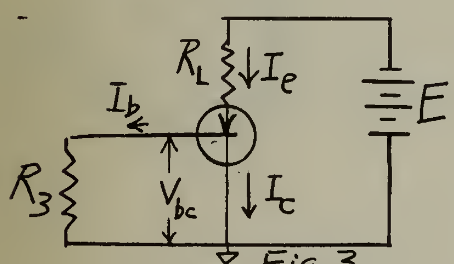

Fig. 3

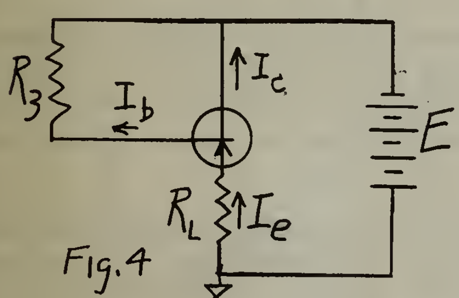

Fig. 4

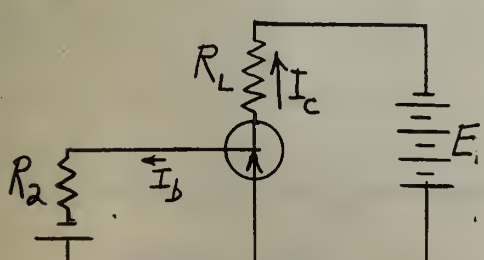

Fig. 5

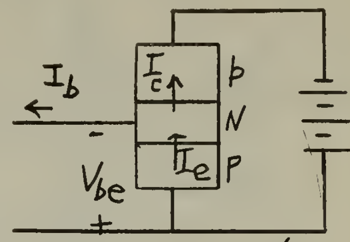

Fig. 6

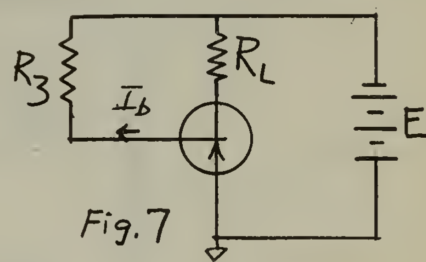

Fig. 7

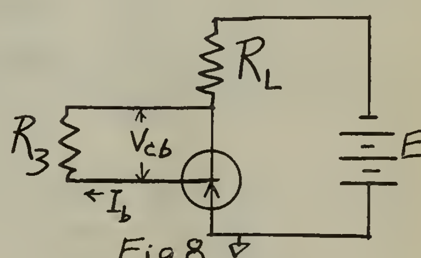

Fig. 8

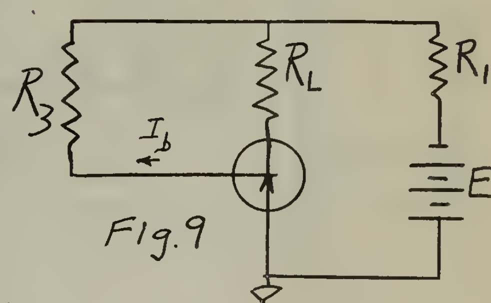

Fig. 9

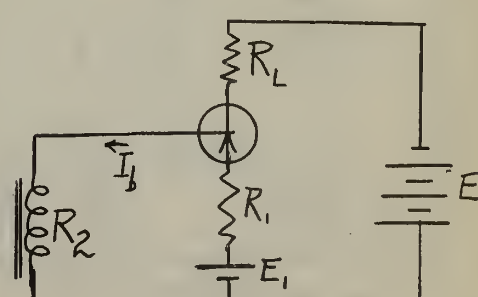

Fig. 10

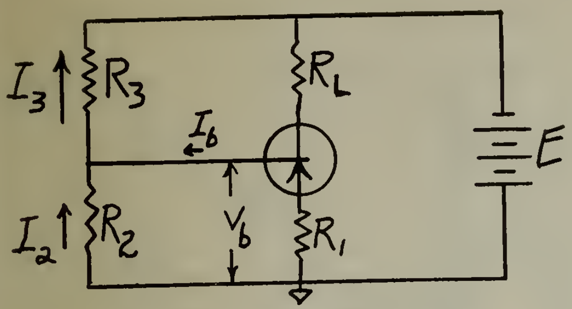

Fig. 11

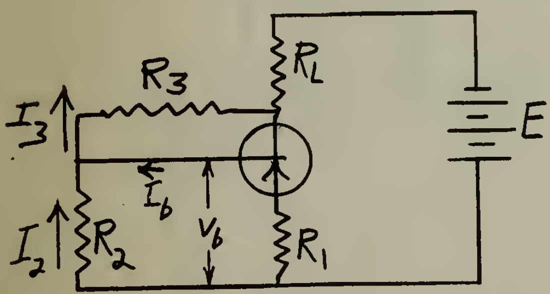

Fig. 12

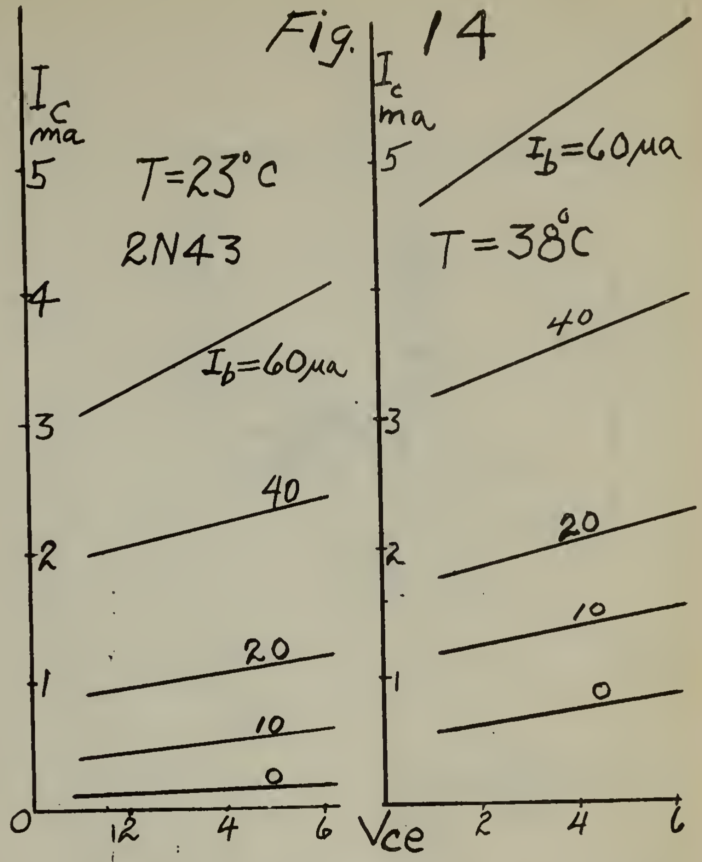

Fig. 14

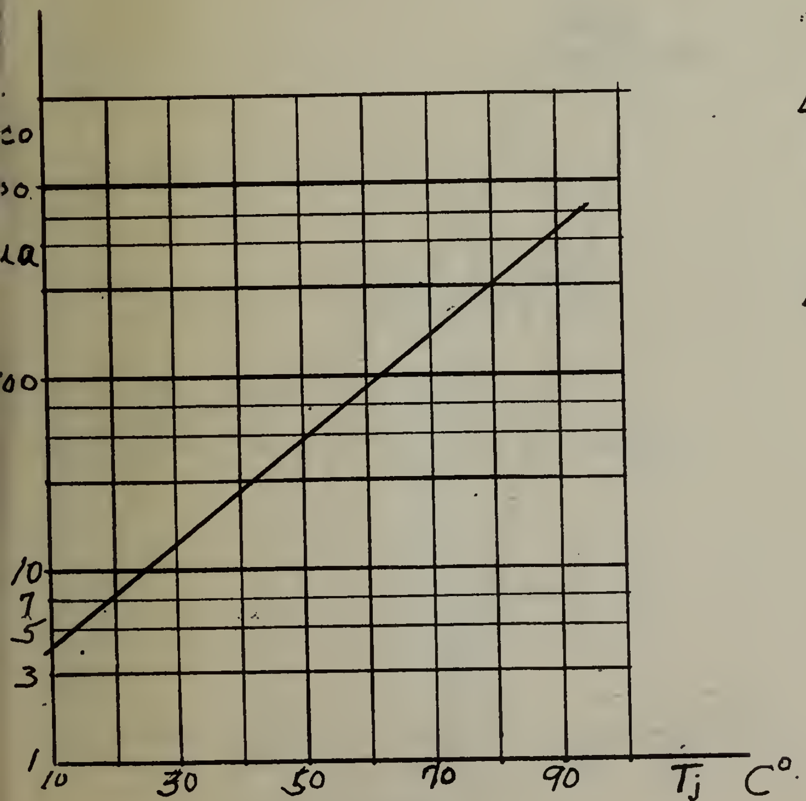

Fig. 13

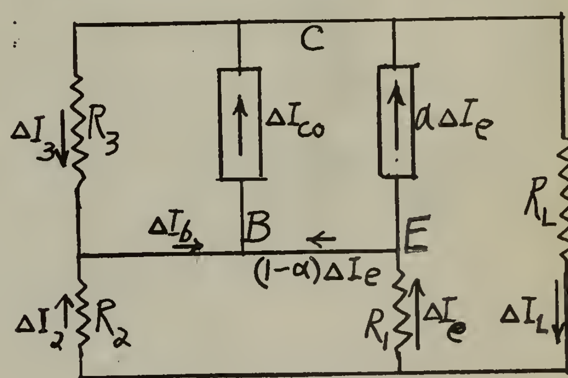

Fig. 15

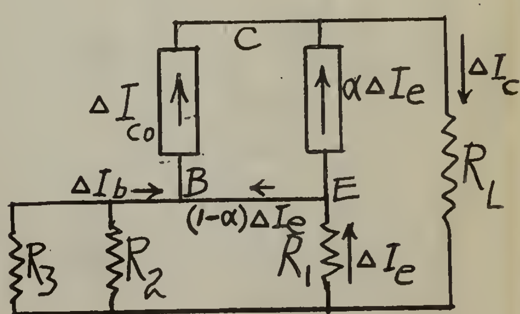

Fig. 16

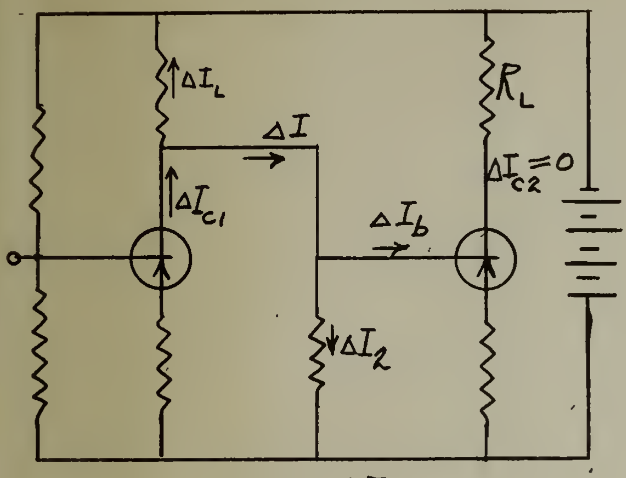

Fig. 17

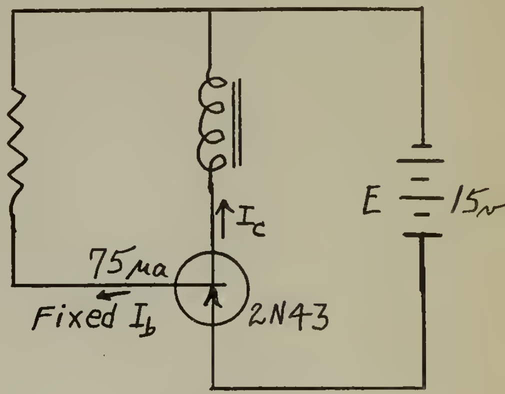

Fig. 18

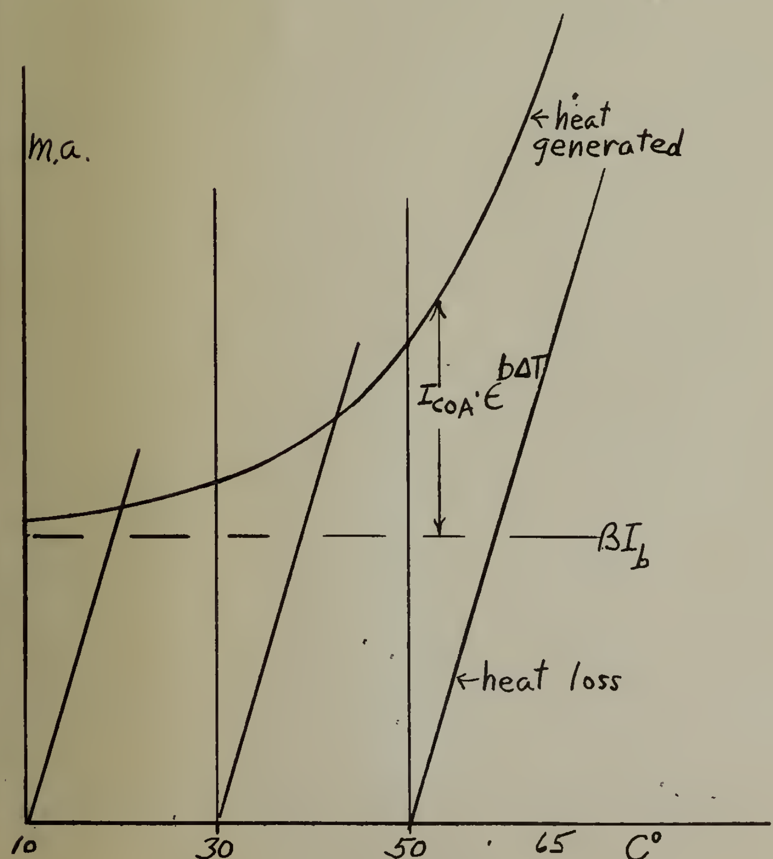

Fig. 19

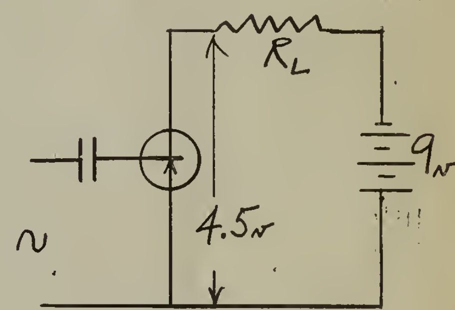

Fig. 20

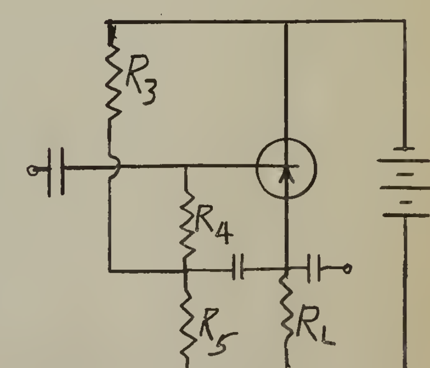

Fig. 21

CC 561
NO 463
27 JAN 66
31 OCT 66
2 JUL 70

11423
13041
12991DUP
14819
14951
18776

TA7 36609
.U6 Bauer
no.17 Transistor bias circuits.